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All Digital Implementation of Dual Mixer Time Difference Technique for Precise Phase and Frequency Measurement

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Abstract

At National Physical Laboratory India, we have developed a precise phase and frequency measurement system as an alternative to the traditional analog approach in order to measure the time differences between the microwave frequency standards and the ensemble of time scale. We have successfully validated the performance of the system and now we are working towards the complete implementation of fully digitized time scale. In this paper we will discuss about the noise floor performance and the possibility for multichannel expansion of the system without affecting the performance. All digital implementation of dual mixer time difference technique is a step towards more precise measurement and evaluation of frequencies and will provide better stability to the timescale. The Allan deviation of the system noise floor stability so far we have achieved for dual channel configuration is $\sigma_{TotalMod}(\tau) = 6 \times 10^{-11} \times \tau^{-1.5}$.

1. Introduction

Time scale is basically an ensemble of clocks where the time evolution of the clock signals are continuously measured and fed to a weighing algorithm to compute the scale. Ensemble of clocks in a time scale basically comprises high stability atomic clocks along with high resolution of measurement system. A simple way to measure frequency is using a frequency counter. But the main problem with such counters is the measurement time. For better resolution we need to measure for a longer time. Time interval counter method and heterodyne methods have been adopted for better resolution but they have their own limitations. Dual mixer time difference (DMTD) [1-2] technique overcomes limitations of most of existing methods of phase and frequency measurement. The conventional DMTD has poor noise performance over long term averaging time because of its analog nature. A time-difference measurement system is simply a phase-difference measurement system that has expanded its capability beyond the modulo-2π limitation. We have mentioned earlier that in time scale measurement clock difference is directly measured and the stability of each clock is then directly fed to a weighing algorithm to compute the time scale. During this measurement the time duration between two consecutive measurement cycles is fairly large. For example the present algorithm of UTC (NPLI) time scale computes the phase differences between the clocks at once in every half an hour i.e. 1800 seconds which allows each measurement to last for a full second or more. Also the measurement system integrated in a time scale must not lose continuity of operation over its lifetime which is often in the order of decades. Therefore any variation of delays in the measurement path in long term basis is not acceptable in time scale computation. But in order to keep the delays constant over longer measurement time is hard to achieve as the performance of the analog ICs present in the measurement system changes over time temperature and other external parameters. This results random walk noise in long term measurement. To overcome it the number of analog components should be reduced in the measurement system without affecting the overall system performance. Keeping it in mind at CSIR NPL, all-digital measurement system has been developed as an alternative to the traditional measurement approach, and a work towards a full implementation of an all-digital time scale is being carried out.
In this paper we will discuss about the technique of phase and frequency measurement based on the DMTD principle but completely digital in nature and its noise floor performance in long term basis.

2. Design Architecture

The detailed design architecture of the all-digital DMTD is shown in figure 1. The key concept of the all-digital implementation is based on the down conversion done by analog to digital converter using digital under sampling technique [4, 5, 6]. Like the mixers in under sampling technique the sampled signal has also a constant phase relationship with the input signal. Then the down converted signal is acquired by a high speed real time data acquisition system. All the data processing including zero crossing detection, time tagging etc. is done completely in digital domain.

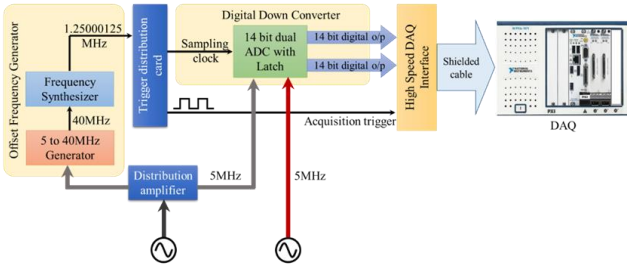

Figure 1: Design Architecture

From figure 1 it is clear that the complete ADDMTD system consists of basically three parts viz. a) A Sub-sampler card which generates the digitized low frequency beat node, b) A precisely tunable offset frequency generator card and c) Distribution amplifier for ADCs and acquisition clock pulses. In addition to these there is a high speed real-time data acquisition system (DAQ) to acquire the low frequency beat node. All the electronic submodules needs to be properly shielded to achieve the optimum performance of the system. The sub-sampler card basically consists of a 14bit high speed ADC. Special care is taken to design the PCB module to avoid any cross talks between the channels. The individual modules are then separately tested and integrated. Till now we have tested the system in a dual channel configuration. But the design architecture is such that the number of channels can be expanded at any point of time without affecting the system performance.

3. Preliminary results and noise floor evaluation

Once we have integrated the complete system we stated rigorous evaluation of the system. The detailed experimental setup is shown in figure 2.

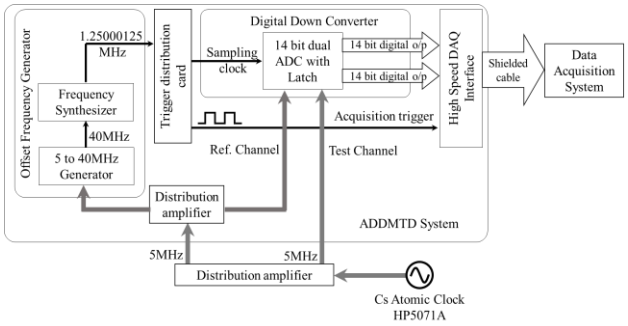

Figure 2: Experimental setup for noise floor performance in dual channel configuration

During this measurement we have connected 5MHz output from Cs Atomic clocks (HP5071A) to the sub-sampler card. Then the digitized beat node (5Hz in our case) is acquired, stored and time tagged by the high speed DAQ. The result is shown in figure 3.

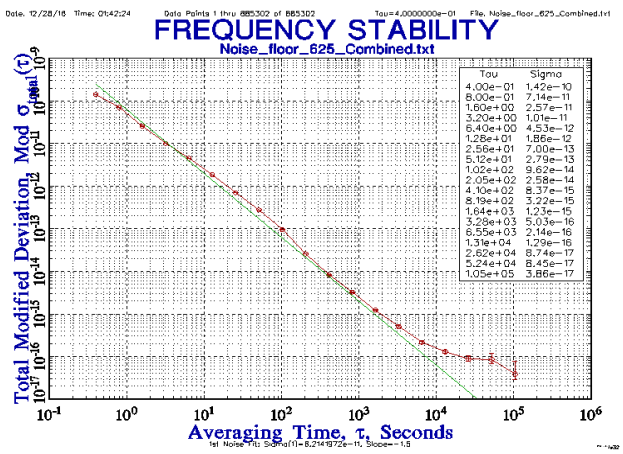

Figure 3: Noise floor performance of the system. Typical stability is $\boldsymbol{\sigma_{TotalMod}(\tau) = 6 \times 10^{-11} \times \tau^{-1.5}}$

6. Conclusion

In this paper a new digital system for precise phase and frequency measurement for time scale computation has described. Due to the instantaneous sampling (sub-sampling) the short term stability of the system is poor than existing commercial instruments. But in case of long term measurement interval the system shows a very good noise performance than the others. The Allan deviation stability of the system noise floor so far we have achieved is $\sigma_{TotalMod}(\tau) = 6 \times 10^{-11} \times \tau^{-1.5}$Therefore it is clear that for stability analysis of precision clocks in time scales the system has wide applications as the long term performance of the system is not dominated by random walk noise. We have successfully tested the dual channel configuration and now we are working towards multi-channel implementation for all digital time scale measurement.

6. Acknowledgements

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7. References

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