# Low Noise L band PLL-VCO designed for the IRNSS -Rx using BiCMOS 180 nm Process

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***Abstract ---A Low Noise L band PLL-VCO designed for the IRNSS–Rx using Sbc18h2 180 nm BiCMOS SiGe 180 nm Process.***

***A SiGe HBT (heterojunction bipolar transistor) BiCMOS process have been used for the very low noise VCO design. NPN transistors based cross coupled architecture have been used for the low noise VCO design. Complete PLL integration with VCO have been designed and tested. Very good phase noise has been achieved from the BiCMOS based VCO. PLL is successfully locked and working. The designed BiCMOS PLL is not only giving the better phase noise performance but also better spurious rejection in the locked condition have been achieved.***

## 1. INTRODUCTION

Voltage controlled oscillator are an integral part of many high frequency analog and clock signal generation systems.These VCO designed generally embedded in a phase-locked system. RF subsystems always demands for the low phase noise VCO. A SiGe HBT (heterojunction bipolar transistor) BiCMOS process have been used for the design of the very low noise VCO.

## 2. DESIGN DESCRIPTION

For this SBC18h2 180 nm SiGe process have been used which has the Ft of around 200 GHz. The used HBT process modules are designed to offer a significant performance gain for this one device as compared with other existing SiGe BiCMOS technologies. Very low noise PLL using VCO designed in the 180 nm SiGe BiCMOS Process have been designed.

For the integration of the PLL modules vz. PFD, Charge pump, prescalar various buffers have been designed.

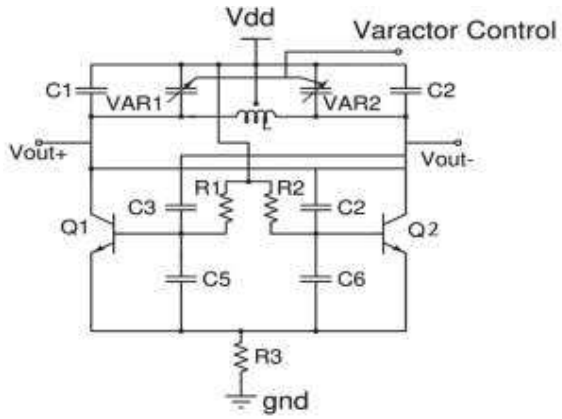


Fig.1 Schematic of the Low Noise VCO designed using HBT based NPN Transistors

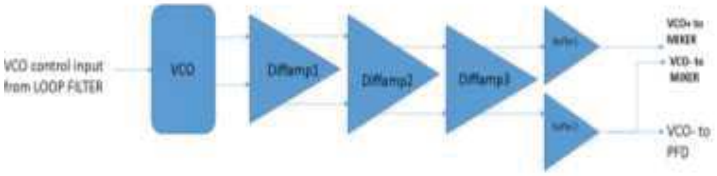


Fig.2 Block diagram of HBT based differential VCO

## 3. DESIGN METHODOLOGY

### 3.1 VCO:

By utilizing the HBT process low phase noise VCO have been designed. A cross coupled NPN transistor pair Q1 & Q2 is used for the negative -Gm implementation. For the Frequency tunning MOS transistor based varactor bank VAR1 and VAR2 have been implemented. MOS varactors provides better supply noise rejection and also less affected by the tank voltage. Use of high Q Differential Inductor L not only make the layout more compact, but also improves the phase noise performance of the VCO. The MIM capacitors C3 and C2 reduces the effect of $C_{bc}$ by providing

negative miller capacitance. The MIM capacitors C5 and C6 enhance the negative resistance and improves the phase noise performance. C1 and C2 are fixed MIM type capacitors calculated as per the are required L-band free running frequency of the VCO. HBT based differential Cascode amplifier in the second stage of the VCO has been implemented before interfacing the VCO with the CMOS based differential amplifiers. The equivalent resistance of the cross coupled pair is -2/gm and hence, it will be necessary that Rp ≥ -1/gm, so that the circuit can behaves as a feedback system with the negative resistance in parallel with the lossy tank. This VCO is called as the negative Gm Oscillator. The fully integrated VCO occupies an active area of 0.6 mm x 1mm.

3.2 PLL:

VCO has been integrated with the respective PLL blocks PFD, charge pump, prescalars, Loop filter with the division factor of the 72. PLL is the 2nd order type has been designed in order to lock the reference frequency of the 16.36 MHz. Multiples analog and digital buffers have been added to achieve the integrated performance.
Designed PLL is 2nd Order System with passive external loop filter.

Natural frequency

$$\omega_n = \sqrt{\frac{K}{\tau_1}}$$

Dumping factor

$$\xi = \frac{1}{2}\sqrt{\frac{K}{\tau_1}}\left(\frac{1}{K} + \tau_2\right)$$

Time constants

$$\tau_1 = \frac{K}{\omega_n^2} \qquad \tau_2 = \frac{2\xi}{\omega_n} - \frac{1}{K}$$

*Integration of the PLL has been done as per the Fig shown below.*

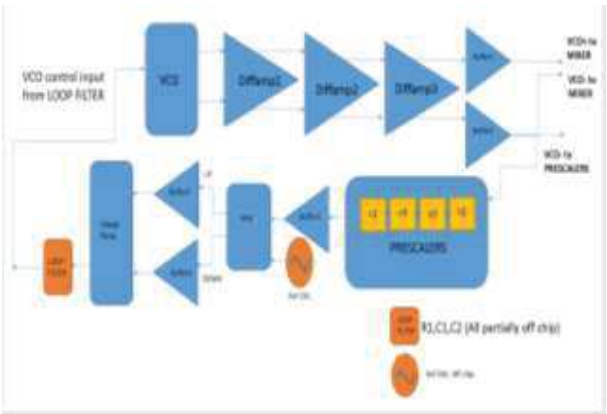


*Fig.3 Integrated PLL block diagram*

Loop Filter off chip components are calculated *keeping the keeping the phase margin > 45◦*

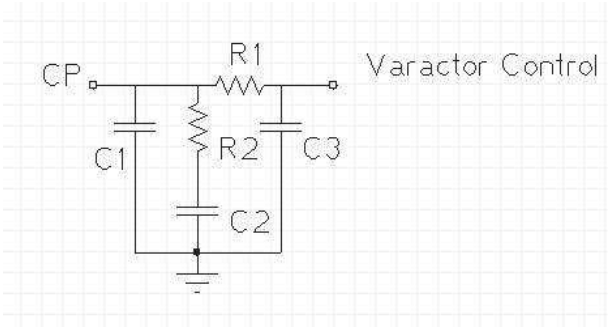


Fig 4. 2nd order Loop filter

## *4 RESULTS AND DISCUSSIONS*

4.1 VCO:

It has been designed with the Cross coupled LC tank based architecture. Successive HBT and CMOS based buffers have been used for the Reverse isolation and Gain. HBT based VCO has been implemented in order to achieve good phase noise performance. VCO has a tuning range from 1.13GHz1.23GHz. KVCO is 2π* 100MHz/0.6 volt. Phase noise is 137 dBc/Hz at the 10MHz offset.

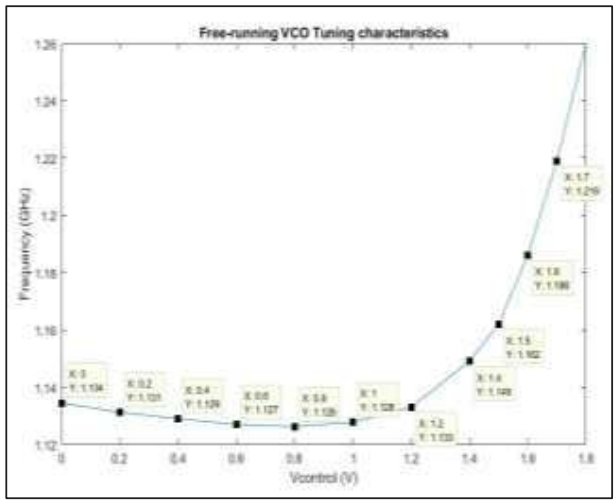


Fig.5 VCO test results Control Frequency Vs Voltage

*PLL:*

VCO has been integrated with the respective PLL blocks PFD, charge pump, prescalars, Loop filter

with the division factor of the 72.PLL is the 2nd order type has been designed in order to lock the reference frequency of the 16.36 MHz. Multiples analog and digital buffers have been added to achieve the integrated performance.

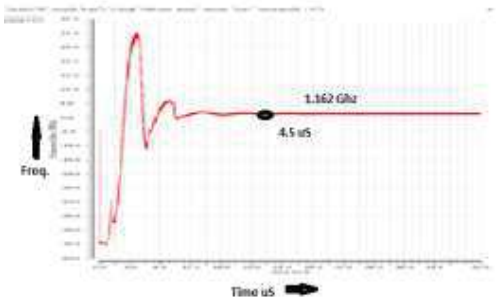


Fig.6 PLL test results Frequency vs Time

*PLL is Locking successfully with the Lock range of 18 MHz*

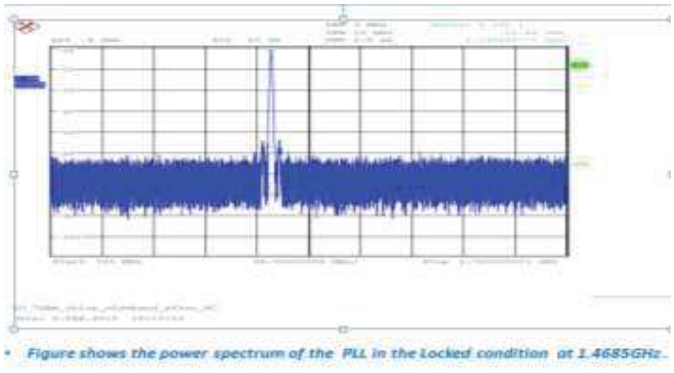


*Fig. 7 Integrated PLL output power vs frequency*


*Fig. 8 Lock range of the Integrated PLL*

*LAYOUT:*

*VCO integrated in the PLL have been fabricated in the 180 nm BiCMOS Towerjazz process. PLL is integrated with the Rx chain in the same chip.*

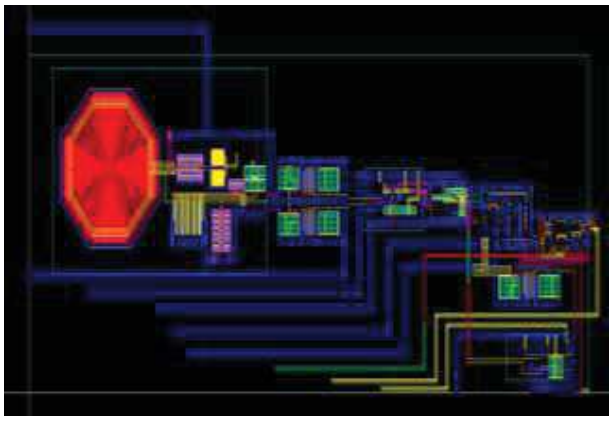

*Fig.9 Layout of the Integrated PLL with the VCO*

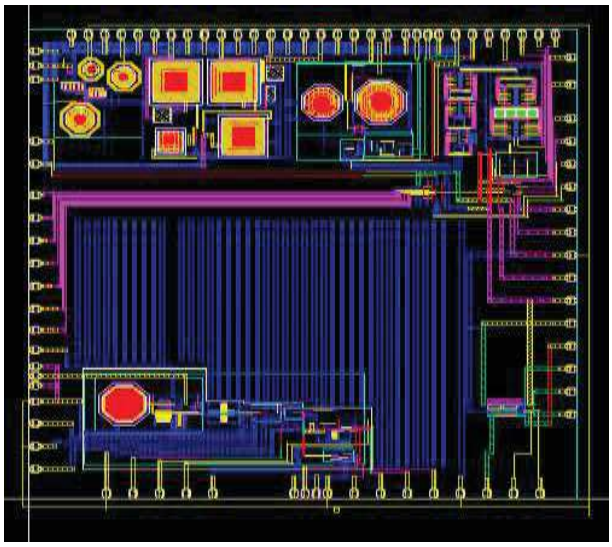

*Fig.10 Layout of the Integrated PLL in the integrated IRNSS -Rx chip*

- *Pin configuration of the Integrated Rx chip with PLL:*

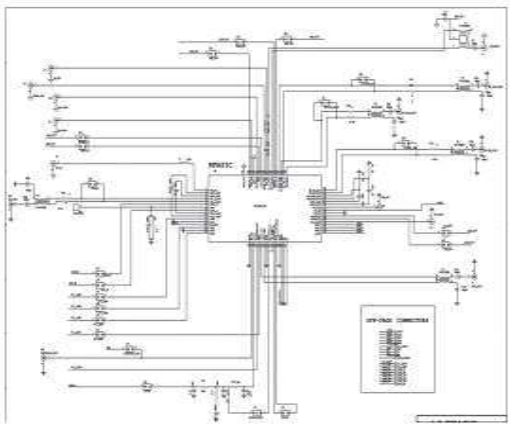

*Fig.11 Integrated IRNSS- Rx Pin details*


*Fig.12 Fabricated dies in BiCMOS 180 nm Towerjazz process*

## 6. CONCLUSION:

Passive inductor based BiCMOS VCO can be used in various RF application with very good phase noise performance using HBT npn transistors. Using the HBT 180 nm SiGe BiCMOS process Low phase noise VCO has been designed and tested using very high Q inductors and performance is fully matched with the simulations.

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He is responsible for system design, planning and development of all Microwave Remote Sensing Payloads of ISRO. He has 2 granted patents, 6 pending patents,5 copyrights and more than 25 papers to his credit. He is the Ex. SAC director and working presently as a Senior Advisor ISRO, Head Quarter. He was the Project Director of RISAT project (Radar Imaging Satellite) of ISRO.During the course of RISAT realisation, he brought the concept of core radar electronics which can be suited to a radar payload with mostly software modifications. In fact, all the payloads of DMSAR, RISAT and Scatterometer share same electronics with different versions of software. H**e can be reached at:**misratapan@sac.isro.gov.in